REMARKS

Claims 1, 5, 26, and 30 are currently pending in the application.

Claims 8, 12, 33, and 37 have been canceled in this amendment.

This amendment is in response to the Office Action of December 8, 2003.

35 U.S.C. § 112 Claim Rejections

Claims 1, 5, 8, 12, 26, 30, 33 and 37 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant has amended claims 1, 5, 26, and 30 clearly comply with the provisions of 35 U.S.C. § 112, first paragraph.

Claims 1 and 26 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant has amended claims 1, 5, 26, and 30 clearly comply with the provisions of 35 U.S.C. § 112, second paragraph.

In summary, Applicant has amended the claimed invention as suggested in the Office Action for the presently claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claims 1, 5, 26, and 30 are allowable under the provisions of 35 U.S.C. § 112.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Eide (U.S. Patent 5,313,096) in view of Kohno et al. (U.S. Patent 5,293,068) and Lin et al. (U.S. Patent 5,239,198)

Claims 1 and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide (U.S. Patent 5,313,096) in view of Kohno et al. (U.S. Patent 5,293,068) and Lin et al. (U.S. Patent 5,239,198).

After considering the cited prior art, the rejection, and the Examiner's comments, Applicant respectfully traverses this rejection and has amended the claimed inventions to clearly distinguish over any combination of the cited prior art.

Applicant asserts that MPEP § 2141 sets forth four factual inquires regarding any rejection under 35 U.S.C § 103 for determining patentability of a claimed invention there are to be considered which include "determining of the scope and contents of the prior art; ascertaining the differences between the prior art and the claims in issue; resolving the level of ordinary skill in the pertinent art; and evaluating evidence of secondary considerations." When applying such required patentability standards, the basic considerations which apply to obviousness rejections based on 35 U.S.C. § 103 should include the following principles of patent law: "the claimed invention must be considered as a whole; the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and reasonable expectation of success is the standard with which obviousness is determined." *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

Applicant further asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

With regard to Claims 1 and 26 which are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide in view of Kohno et al. and Lin et al., Applicant respectfully submits that the rejection of such claims based upon such a combination of the cited prior art does not meet the requirements of the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; the references must be

viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and reasonable expectation of success is the standard with which obviousness is determined as set forth at the end of the second preceding paragraph in her consideration of the references. Furthermore, Applicant asserts that any such combination of the cited prior art fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claims 1 and 26.

As stated in the Office Action, Eide does not teach that the plurality of bond pads extend along a longitudinal axis. Kohno teaches a plurality of bond pads extending along a longitudinal axis of a die on a surface of the die. It was asserted that it would have been obvious to use the longitudinal layout of bond pads of Kohno in the method of Eide in order to simplify a layout of bond pads. Eide and Kohno do not teach connection of the second substrate to a first substrate, or a plurality of bond pads located on the second attachment surface and on the die side of the second substrate. Also, as stated in the Office Action it is asserted that it would have been obvious to use the plurality of bond pads of the second substrate, the entire first substrate, and connecting of Lin in the method of Eide and Kohno in order to provide external electrical connections to the device as stated by Lin in column 2, lines 44—50.

Applicant asserts that when modifying one piece of prior art with another to arrive at the conclusion that the combination is obvious, "the proposed modification cannot render the prior art unsuitable for its intended purpose." MPEP 2104.01.

Turing to the cited prior art, Eide is directed to an IC chip package having an upper active surface bonded to the lower surface of a lower layer of a combination of a lower layer and an upper layer adhesively bonded together forming one of the substrates of the IC chip package with the chip package being encapsulated after attachment to a lead frame or substrate (See FIG. 11). A plurality of terminals on the active surface are wire bonded within the outer periphery of the chip by bonding wires extending through a plurality of apertures in a lower layer of the substrate to bonding pads on an upper surface of the lower layer of the substrate. Metalized strips couple the bonding pads to conductive pads at the outer edges of the lower layer of the substrate. The substrate includes an upper layer having apertures therein. After wire bonding, the apertures in the upper and lower substrate layers are filled with epoxy which is cured and then ground flush

with the upper surface of the upper layer of the substrate. It should be noted that an upper layer and a lower layer are required by Eide to form the substrate having a semiconductor die mounted thereon on the lower surface only thereof. Also, Eide only has bond wires extending through the aperture in the lower layer of substrate while extending into but not through the aperture in the upper layer of the substrate. (See FIG. 6) Further, Eide has all solder strips of all substrates connected to the same conductive pads on substrates 12 and connected to a lead frame or substrate 14. It should be noted that the upper layer 26 of the substrate 12 does not contain circuitry thereon but, rather, a plurality of conductive pads 30 connected to conductive pads 30 of the lower layer 24 of the substrate 12 by way of conductive strips 28. (See FIG. 2.) After forming the stack of substrates and semiconductor die, the stack is solder dipped and encapsulated. (See FIG. 11, steps 118, 120.) Eide contains no disclosure, teaching or suggestion but the use of a lower layer 24 and an upper layer 36 forming the substrate 12. Eide further locates the semiconductor die 20 below the lower layer 24 of the substrate 12 in the chip stack 10. Nowhere in Eide is there any disclosure, teaching or suggestion of attaching a semiconductor die 20 except below the lower layer 24 of the substrate 12. There is no disclosure, teaching, or suggestion whatsoever in Eide for inverting the lower layer 24 of the substrate 12 and attaching an upper layer 26 for form the substrate 12. Nowhere in Eide is there any description, teaching, or suggestion regarding the presently claimed invention of a method of forming a wire bond style/flip chip attach assembly . . . of presently amended independent claims 1, 5, 26, and 30.

Kohno is directed to an encapsulated semiconductor device having a chip, a chip pad having through holes and also conducting patterns corresponding to an electrode pad of the chip and leads. An arbitrary external terminal arrangement is obtained by combination of a wire bonding operation between the conducting pattern and lead. After the device has been fabricated, the entire device (semiconductor die 1, substrate 2, and portions of leads 6) is encapsulated by a resin 7 . (See Kohno, column 5, lines 42, 43.) In FIG. 3 of Kohno, a portion of the resin 7 has been remove and a plane of the device positioned opposite to a printed circuit board is arranged upwardly. (See kohno, column 5, lines 47—55.) Nowhere in Kohno is there any description, teaching or suggestion regarding the presently claimed invention of a method of forming a wire

bond style/flip chip attach assembly . . . of presently amended independent claims 1, 5, 26, and 30.

Lin is directed to a multiple chip semiconductor device in which a first pattern of conductive trances is formed on one surface of a substrate and a second pattern of traces is formed on a second surface of the substrate. A fist semiconductor die is interconnected to the first traces and a package body is formed around the first die and a portion of the traces. A second semiconductor die is interconnected to the second traces on the second surface. A second package body is formed around the second die and a portion of the traces. Solder balls are coupled to exposed portions of the second traces around the perimeter of the package body to establish power and ground connections to each die. A plurality edge leads are externally soldered to the traces around the periphery of the substrate to establish remaining electrical connections in addition to the power and ground connections of the solder balls to the traces. Nowhere is there any description, teaching or suggestion regarding the presently claimed invention of a method of forming a wire bond style/flip chip attach assembly . . . of presently amended independent claims 1 and 26 in Lin.

Applicant asserts that the only suggestion whatsoever for the presently claimed invention of presently amended independent claims 1 and 26 is solely Applicant's disclosure, not the cited prior art which is required for any rejection under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. Applicant asserts that nowhere in any combination of Eide and Kohno and Lin is there any description, teaching or suggestion regarding the presently claimed invention of a method of forming a wire bond style/flip chip attach assembly . . . of presently amended independent claims 1 and 26 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention.

Applicant asserts that there is no reason whatsoever to modify Eide as suggested in the Office Action to use the longitudinal layout of bond pads of Kohno in the method of Eide in order to simplify a layout of bond pads. Applicant asserts that if the layout of the bond pads in Eide is to be simplified, all that needs to be done is to use one end of the semiconductor die 20 and have all bond pads placed thereon so that only one aperture is needed in the upper layer forming a portion of the substrate 12. Applicant asserts that there is no reason whatsoever to use

Kohno or Lin for any teaching or suggestion except in a hindsight reconstruction of the Applicant's claimed invention based solely upon Applicant's disclosure.

Further, Applicant asserts that if Eide is modified as suggested in the Office Action the Eide device is destroyed because Eide does not have any inverted semiconductor die 20 attached to either the lower layer 24 or upper layer 26 of the substrate 12. Applicant asserts that any modification of Eide does not result is not the presently claimed inventions of presently amended independent claims 1 and 26. The Eide chip stack 10 is not directed to the presently claimed inventions of presently amended independent claims 1 and 26 of a method of forming a wire bond style/flip chip attach assembly. The Eide substrate 12 comprises a lower layer 24 and an upper layer 26 to form the substrate 12. In any modification of the Eide substrate 12 based upon any teachings or suggestions of Kohno to substitute the substrate 2 and chip1 arrangement therefrom to modify Eide, the Eide substrate must always still contain a lower layer 24 and an upper layer 26. Otherwise, the Eide invention is destroyed because Eide relies upon having two layers in the substrate for circuitry, for connections to other substrates having semiconductor die to form the chip stack 10, and to allow for the grinding of both the upper surface 22 of the upper layer 26 of the substrate 12 and the bottom surface of the semiconductor die 20 for precise thickness control of the substrate 12 and semiconductor die 20. Any modification to the Eide substrate and semiconductor die 20 must always use a lower layer and upper layer substrate 12 for the Eide invention to function in its intended manner. If the substrate 2 and semiconductor die 1 of Kohno are to be used to modify the Eide substrate 12 and semiconductor die 20, it is speculation as to how they are to be modified because Kohno teaches or suggests a single layer substrate 2 having a semiconductor die 1 thereon being encapsulated in resin 7 to form a package. The Eide chip stack 10 contains no encapsulation, except to fill an aperture in the upper layer 26 of the substrate. If it is attempted to merely modify the substrate 12 and semiconductor die 20 of Eide to be a single layer substrate 2 and semiconductor die 1 based upon any teaching or suggestion of Kohno, the bond wires 72 of Eide either protrude above the upper surface 22 of the substrate 12 or protrude below the lower surface 42 of the substrate 12 making it impossible to form a chip stack 10, the invention of Eide.

Further, if Eide is to be modified based upon a teaching or suggestion of Lin, Applicant asserts that the Eide chip stack is destroyed. Lin uses both edge leads 36 and solder balls 32 to connect between the substrate 12 and both semiconductor die 20 and 27 located thereon and conventional substrate 38. Eide uses solder strips 16 to connect between substrates 12 of the chip stack 10. Eide contains no teaching or suggestion to use any connector but solder strips 16. Lin contains no teaching or suggestion but the use of both edge connectors 36 and solder balls 32. Again, Applicant asserts that it is speculation as to how Eide is to be modified to replace solder strips 16 with solder balls 32 and/or edge connector 36. Applicant asserts that since Eide uses edge connectors 28 between the lower layer 24 and upper layer 26 of the substrate 12 that edge connectors 36 of Lin would be used for the connectors 28.

If the teachings or suggestions of the Konho substrate and semiconductor die are used to modify the Eide substrate and semiconductor die stack, the Kohno substrate and semiconductor die are substituted for the lower layer 26 of the Eide substrate 12. In such an instance, the semiconductor die 20 is located on the upper side of the lower layer 24 of the substrate 12 which requires that the upper layer 26 of the substrate 12 be modified to include an aperture for an encapsulated semiconductor die and entire upper surface being covered with resin 7, if possible, and that the bond wires 4w of Kohno extend below the lower layer 24 of the substrate 12 of Eide being encapsulated in resin 7 covering the entire lower surface of the lower layer 24 of the substrate 12 and the entire upper surface of the lower layer 24 resulting in all bond pads 48 of Eide being covered with resin 7 so that no connections can be made thereto by any connection method using any connector. Such a combination of Eide and Kohno is inoperative and clearly destroys any function of the Eide assembly. Such is not the presently claimed invention which has the semiconductor die mounted above the adapter board or adapter substrate, not mounted on the lower substrate 24 of the substrate 12;i.,e. an inverted arrangement, with the bond pads of the semiconductor die 1 being covered by portions of the lower substrate so that wire bonding connections between the circuits on the and the semiconductor die on the upper substrate are impossible. In Eide the substrate 12 is composed of two substrates having different thicknesses, lower substrate 24 and upper substrate 26, adhesively secured to each other with the upper

surface 64 if the upper substrate 26 being ground flat after filling of the apertures 58 and 60 therein with epoxy.

Yet further, as stated in the Office Action, Eide and Kohno do not teach connection of the second substrate to a first substrate, or a plurality of bond pads located on the second attachment surface and on the die side of the second substrate.

The teaching or suggestion of Eide is to eliminate the waste of space among semiconductors attached to a substrate. Col. 1. lines 65-68, Col. 2 lines 1-2, lines 29-32. Eide specifically rejects the "outward" lead configuration of Fig. 9 in favor of his own "inward" lead configuration (Fig. 10) which "provides for substantially greater chip density within the chip stack." Col. 6, line 68. Taking the idea of axial bond placement from Kohno would inevitably lead to the space-inefficient "outward" lead configuration. Therefore the combination of Eide with Kohno is improper and cannot establish a *prima facie* case of obviousness under 35 U.S.C. 103 because they teach away from any combination thereof and destroy the invention of Eide.

Additionally, "the references must suggest the desirability and thus the obviousness of making the combination. As set forth above, the combination of Eide and Kohno do not, let alone additionally teach their combination with Lin. Furthermore, Lin does not suggest its combination with the lead frame 14-to-semiconductor die 20 attachment of Eide with or without the axial bond placement of Kohno.

Yet further, "the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." As set forth above, Applicant's invention pertains to making an adaptor board which interconnects semiconductors and board elements. Lin does disclose a board-to-board connection, but it is only with the hindsight provided by Applicant's disclosure that the elements of the cited prior art are randomly picked and chosen for specific, relevant characteristics (connecting said second substrate to said first substrate having said second located solely on one side of said first substrate without any portion of said first substrate being located below said upper surface of said second substrate and portions of said plurality of bond wires extending between the second attachment surface of said second substrate and a surface of said first substrate, the connections between said first substrate and said second

substrate formed by one of a plurality of solder balls and a plurality of pins) from the myriad of teachings or suggestions in Lin's Fig. 4.

For example, in Fig. 4, Lin also discloses putting traces on both sides of the second substrate. The two types of traces are electrically connected. Both types of traces are connected to the board. There are semiconductor die on both sides of the board. The die are packaged. The packaging occludes part of the surrounding traces. In short, it is from this complex picture that specific elements of the claimed invention are randomly picked and chosen and then combined with other teachings to reconstruct the claimed invention.

Nowhere in the Office Action is a *prima facie* case of obviousness under 35 U.S.C. 103 established meeting all the criteria as set forth herein. As set forth above, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Claims 1 and 26 are allowable.

Still yet further, any combination of the cited prior art Eide and Kohno and Lin does not teach or suggest the claim limitations of the presently claimed inventions of claims 1 and 26. Any combination of the cited prior art fails to teach or suggest the claim limitations of the presently claimed inventions of claims 1 and 26 calling for "[a] method of forming a wire bond style/flip chip attach assembly electrically connecting a semiconductor die having a bond pad pattern to a first substrate having a connector pattern arrangement when said semiconductor die is attached to second adapter substrate having an upper surface and having a second surface having a connector pattern thereon", "providing an inverted bare semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said semiconductor die on said surface in a first bond pad pattern different than the connector pattern arrangement of the first substrate", providing a second adapter substrate having a die side surface, a second attachment surface, at least one via extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface having a connector pattern connected to the plurality of circuits matching the connector pattern arrangement of the first substrate and a plurality of bond pads located in a first bond pad pattern connected to the plurality of circuits matching the first bond

pad pattern of the bare semiconductor die", "applying an adhesive to a portion of the die side of the first substrate to attach the inverted bare semiconductor die thereto", "attaching a portion of the surface having a plurality of bond pads thereon of the inverted bare semiconductor die to a portion of the die side surface of said second substrate locating the bare semiconductor die above the second adapter substrate having the bond pads of the semiconductor die located over the via in the second adapter substrate", "connecting said plurality of bond pads of the inverted bare semiconductor die to said plurality of bond pads on the second attachment surface of said second adapter substrate using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending from bond pads of the semiconductor die located on the die side surface of the second adapter substrate through said second adapter substrate to the second attachment surface of the second adapter substrate, the plurality of wire bonds connected to the first bond pad pattern of the inverted semiconductor die and to the matching first bond pad pattern on the second attachment surface of the second adapter substrate", "connecting said second adapter substrate to said first substrate having said second substrate located solely on one side of said first substrate, the connections between said first substrate and said adapter second substrate formed by a plurality of adapter board connectors extending between the matching connector pattern on the second attachment surface of the second adapter substrate to the connector arrangement of the first substrate", a "method of forming a wire bond style/flip chip attach assembly attaching a semiconductor die having a first bond pad pattern to a first substrate having a connector pattern arrangement for attaching said first substrate to a second adapter substrate having an upper surface and having a second surface having a connector pattern thereon and having a plurality of circuit traces thereon", "providing an inverted bare semiconductor die having a surface having a plurality of bond pads located along a longitudinal axis of said die on said surface [and a semiconductor die having a surface having at least one bond pad] extending in a leads-over configuration on said surface, the plurality of bond pads having a first bond pad pattern different than the connector pattern arrangement of the first substrate", "providing a second adapter substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the

second adapter substrate having a connector pattern thereon connected to the plurality of circuits matching the connector pattern arrangement of the first substrate and a plurality of bond pads connected to the plurality of circuits in a bond pad pattern matching the first bond pad pattern of the inverted bare semiconductor die", "filling a potion of the via in the substrate with a sealant] applying an adhesive to a portion of the die side of the substrate to attach the inverted bare semiconductor die thereto", "attaching a portion of the surface having a plurality of bond pads thereon of the bare semiconductor die to a portion of the die side surface of said second substrate", "connecting said plurality of bond pads of the inverted bare semiconductor die to said plurality of bond pads of said second adapter substrate using a plurality of bond wires, said plurality of bond wires extending through said at least one via extending through said second adapter substrate, the plurality of bond wires connected to the first bond pad pattern of the plurality of bond pads of the inverted semiconductor die and to the matching first bond pad pattern of the plurality of bond pads on the second attachment surface of the second adapter substrate", and "attaching said first substrate to said second attachment surface of said second adapter substrate using a plurality of adapter board connectors extending from the second attachment surface of the second adapter substrate".

Applicant asserts that since any combination of the cited prior art fails to teach or suggestion the claim limitations of the presently claimed invention of claims 1 and 26 as set forth herein, any combination of the cited prior art fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of presently amended independent claims 1 and 26.

Additionally, Applicant asserts that the only possible rejection of presently amended independent claims 1 and 26 based upon any combination of the cited prior art would be a hindsight reconstruction of the presently claimed invention based solely upon the teachings and suggestions of Applicant's disclosure, not the cited prior art. Such a rejection is neither contemplated by nor within the ambit of 35 U.S.C. 21 103 and, clearly, improper.

Therefore, presently amended independent claims 1 and 26 are allowable.

Obviousness Rejection Based on Eide (U.S. Patent No. 5,313,096) in view of Lin et al. (U.S. Patent No. 5,239,198)

Claims 5 and 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide (U.S. Patent 5,313,096) in view of Lin et al. (U.S. Patent 5,239,198). Applicant respectfully traverses this rejection, as hereinafter set forth.

As previously stated, Applicant asserts that nowhere in any combination of Eide and Kohno and Lin is there any description, teaching or suggestion regarding the presently claimed invention of a method of forming a wire bond style/flip chip attach assembly . . . of presently amended independent claims 5 and 30 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention.

Applicant asserts that there is no reason whatsoever to modify Eide as suggested in the Office Action to use the longitudinal layout of bond pads of Kohno in the method of Eide in order to simplify a layout of bond pads. Applicant asserts that if the layout of the bond pads in Eide is to be simplified, all that needs to be done is to use one end of the semiconductor die 20 and have all bond pads placed thereon so that only one aperture is needed in the upper layer forming a portion of the substrate 12. Applicant asserts that there is no reason whatsoever to use Kohno for any teaching or suggestion except in a hindsight reconstruction of the Applicant's claimed invention based solely upon Applicant's disclosure.

Further, Applicant asserts that if Eide is modified as suggested in the rejection the Eide device is destroyed because Eide does not have any inverted semiconductor die 20 attached to either the lower layer 24 or upper layer 26 of the substrate 12, Further, any modification of Eide does not result is not the presently claimed inventions of presently amended independent claims 1, 5, 26, and 30. The Eide chip stack 10 is not directed to the presently claimed inventions of presently amended independent claims 5 and 30 of a method of forming a wire bond style/flip chip attach assembly. The Eide substrate 12 comprises a lower layer 24 and an upper layer 26 to form the substrate 12. In any modification of the Eide substrate 12 based upon any teachings or suggestions of Kohno to substitute the substrate 2 and chip1 arrangement therefrom to modify Eide, the Eide substrate must always still contain a lower layer 24 and an upper layer 26. Otherwise, the Eide invention is destroyed because Eide relies upon having two layers in the

substrate for circuitry, for connections to other substrates having semiconductor die to form the chip stack 10, and to allow for the grinding of both the upper surface 22 of the upper layer 26 of the substrate 12 and the bottom surface of the semiconductor die 20 for precise thickness control of the substrate 12 and semiconductor die 20. Any modification to the Eide substrate and semiconductor die 20 must always use a lower layer and upper layer substrate 12 for the Eide invention to function in its intended manner. If the substrate 2 and semiconductor die 1 of Kohno are to be used to modify the Eide substrate 12 and semiconductor die 20, it is speculation as to how they are to be modified because Kohno teaches or suggests a single layer substrate 2 having a semiconductor die 1 thereon being encapsulated in resin 7 to form a package. The Eide chip stack 10 contains no encapsulation, except to fill an aperture in the upper layer 26 of the substrate. If it is attempted to merely modify the substrate 12 and semiconductor die 20 of Eide to be a single layer substrate 2 and semiconductor die 1 based upon any teaching or suggestion of Kohno, the bond wires 72 of Eide either protrude above the upper surface 22 of the substrate 12 or protrude below the lower surface 42 of the substrate 12 making it impossible to form a chip stack 10, the invention of Eide.

Further, if Eide is to be modified based upon a teaching or suggestion of Lin, Applicant asserts that the Eide chip stack is destroyed. Lin uses both edge leads 36 and solder balls 32 to connect between the substrate 12 and both semiconductor die 20 and 27 located thereon and conventional substrate 38. Eide uses solder strips 16 to connect between substrates 12 of the chip stack 10. Eide contains no teaching or suggestion to use any connector but solder strips 16. Lin contains no teaching or suggestion but the use of both edge connectors 36 and solder balls 32. Again, Applicant asserts that it is speculation as to how Eide is to be modified to replace solder strips 16 with solder balls 32 and/or edge connector 36. Applicant asserts that since Eide uses edge connectors 28 between the lower layer 24 and upper layer 26 of the substrate 12 that edge connectors 36 of Lin would be used for the connectors 28.

If the teachings or suggestions of the Konho substrate and semiconductor die are used to modify the Eide substrate and semiconductor die stack, the Kohno substrate and semiconductor die are substituted for the lower layer 26 of the Eide substrate 12. In such an instance, the semiconductor die 20 is located on the upper side of the lower layer 24 of the substrate 12 which

requires that the upper layer 26 of the substrate 12 be modified to include an aperture for an encapsulated semiconductor die and entire upper surface being covered with resin 7, if possible, and that the bond wires 4w of Kohno extend below the lower layer 24 of the substrate 12 of Eide being encapsulated in resin 7 covering the entire lower surface of the lower layer 24 of the substrate 12 and the entire upper surface of the lower layer 24 resulting in all bond pads 48 of Eide being covered with resin 7 so that no connections can be made thereto by any connection method using any connector. Such a combination of Eide and Kohno is inoperative and clearly destroys any function of the Eide assembly. Such is not the presently claimed invention which has the semiconductor die mounted above the adapter board or adapter substrate, not mounted on the lower substrate 24 of the substrate 12;i.,e. an inverted arrangement, with the bond pads of the semiconductor die 1 being covered by portions of the lower substrate so that wire bonding connections between the circuits on the and the semiconductor die on the upper substrate are impossible. In Eide the substrate 12 is composed of two substrates having different thicknesses, lower substrate 24 and upper substrate 26, adhesively secured to each other with the upper surface 64 if the upper substrate 26 being ground flat after filling of the apertures 58 and 60 therein with epoxy.

Yet further, as stated in the Office Action, Eide and Kohno do not teach connection of the second substrate to a first substrate, or a plurality of bond pads located on the second attachment surface and on the die side of the second substrate.

The teaching or suggestion of Eide is to eliminate the waste of space among semiconductors attached to a substrate. Col. 1. lines 65-68, Col. 2 lines 1-2, lines 29-32. Eide specifically rejects the "outward" lead configuration of Fig. 9 in favor of his own "inward" lead configuration (Fig. 10) which "provides for substantially greater chip density within the chip stack." Col. 6, line 68. Taking the idea of axial bond placement from Kohno would inevitably lead to the space-inefficient "outward" lead configuration. Therefore the combination of Eide with Kohno is improper and cannot establish a *prima facie* case of obviousness under 35 U.S.C. 103 because they teach away from any combination thereof and destroy the invention of Eide.

Additionally, "the references must suggest the desirability and thus the obviousness of making the combination. As set forth above, the combination of Eide and Kohno do not, let

alone additionally teach their combination with Lin. Furthermore, Lin does not suggest its combination with the lead frame 14-to-semiconductor die 20 attachment of Eide with or without the axial bond placement of Kohno.

Yet further, "the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." As set forth above, Applicant's invention pertains to making an adaptor board which interconnects semiconductors and board elements. Lin does disclose a board-to-board connection, but it is only with the hindsight provided by Applicant's disclosure that the elements of the cited prior art are randomly picked and chosen for specific, relevant characteristics (connecting said second substrate to said first substrate having said second located solely on one side of said first substrate without any portion of said first substrate being located below said upper surface of said second substrate and portions of said plurality of bond wires extending between the second attachment surface of said second substrate and a surface of said first substrate, the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins) from the myriad of teachings or suggestions in Lin's Fig. 4.

For example, in Fig. 4, Lin also discloses putting traces on both sides of the second substrate. The two types of traces are electrically connected. Both types of traces are connected to the board. There are semiconductor die on both sides of the board. The die are packaged. The packaging occludes part of the surrounding traces. In short, it is from this complex picture that specific elements of the claimed invention are randomly picked and chosen and then combined with other teachings to reconstruct the claimed invention.

Nowhere in the Office Action is a *prima facie* case of obviousness under 35 U.S.C. 103 established meeting all the criteria as set forth herein. As set forth above, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Claims 1 and 26 are allowable.

Still yet further, any combination of the cited prior art Eide and Kohno and Lin does not teach or suggest the claim limitations of the presently claimed inventions of claims 5 and 30. Any combination of the cited prior art fails to teach or suggest the claim limitations of the

presently claimed inventions of claims 5 and 30 calling for a "method of forming a wire bond style/flip chip attach assembly electrically connecting a semiconductor die having a first bond pad pattern to a master board having a connector pattern arrangement", "providing an inverted bare semiconductor die having a plurality of bond pads located in at least two rows extending down the longitudinal axis of inverted the bare semiconductor die thereon, the at least two rows of bond pads having a first bond pad pattern", "providing a master board having a plurality of circuit traces on an upper surface thereof connected to a plurality of connectors in a second connector pattern arrangement located thereon different than the first bond pad pattern of the plurality of bond pads of the inverted bare semiconductor die", "providing an adapter board having a die side surface, a second attachment surface, a via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, a plurality of bond pads located on the second attachment surface of the board having a plurality of bond pads connected to the plurality of circuits matching the first bond pad pattern of the plurality of bond pads of the inverted bare semiconductor die, and having a connector pattern connected to the plurality of circuits matching the connector pattern arrangement of the plurality of connectors of the master board", "providing a plurality of electrical connectors for connecting the connector pattern connected to the plurality of circuits matching the connector pattern arrangement of the plurality of connectors of the master board located on the second attachment surface of the board to the plurality of connectors in a second connector pattern arrangement of the circuit traces of the master board", "attaching a portion of said inverted bare semiconductor die to a portion of the die side surface of the adapter board", "connecting said plurality of bond pads of said inverted bare semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the via extending through the adapter board having a portion thereof attached to the plurality of bond pads on the second attachment surface of the adapter board and having a portion thereof attached to the plurality of bond pads on the bare semiconductor die", "connecting said adapter board and master board using said plurality of electrical connectors on said adapter board to said plurality of circuit traces on said master board using the plurality of electrical connectors", a "method of forming a wire bond style/flip chip attach assembly attaching a semiconductor die to a master board", "providing an

inverted bare semiconductor die having a plurality of bond pads in at least two rows having a first bond pad arrangement located down the longitudinal axis of a surface of the inverted bare semiconductor die in a leads over chip configuration", "providing a master board having a plurality of circuit traces on an upper surface thereof connected to a plurality of connectors in a connector pattern arrangement located thereon, said upper surface for the receipt of an inverted bare semiconductor die therein", "providing an adapter board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, a plurality of bond pads located on the second attachment surface of the adapter board having a plurality of bond pads connected to the plurality of circuits in a first bond pad pattern matching the first bond pad pattern of the inverted bare semiconductor die, and having a connector pattern thereon connected to the plurality of circuits matching the connector pattern arrangement of the master board;
providing a plurality of electrical connectors for connecting the connector pattern of the plurality of circuits located on the second attachment surface of the adapter board to the plurality of circuits", "attaching a portion of said inverted bare semiconductor die to a portion of the die side surface of the board", "connecting said plurality of bond pads in a first bond pad arrangement of said bare semiconductor die to said plurality of bond pads in a matching first bond pad pattern of said adapter board using a plurality of bond wires extending through the via extending through the board from the die side surface to the second attachment surface", and "connecting said adapter board and master board using said plurality of electrical connectors on said board to said at least one circuit trace on said master board using adapter board".

Applicant asserts that since any combination of the cited prior art fails to teach or suggestion the claim limitations of the presently claimed invention of claims 5 and 30 as set forth herein, any combination of the cited prior art fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of presently amended independent claims 5 and 30.

Additionally, Applicant asserts that the only possible rejection of presently amended independent claims 5 and 30 based upon any combination of the cited prior art would be a hindsight reconstruction of the presently claimed invention based solely upon the teachings and

suggestions of Applicant's disclosure, not the cited prior art. Such a rejection is neither contemplated by nor within the ambit of 35 U.S.C. 21 103 and, clearly, improper.

Therefore, presently amended independent claims 5 and 30 are allowable.

Obviousness Rejection Based on Kryzaniwsky (U.S. Patent 5,099,309) in view of Kohno et al. (U.S. Patent 5,293,068) and Lin et al. (U.S. Patent 5,239,198)

Claims 8, 12, 33 and 37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (U.S. Patent 5,099,309) in view of Kohno et al. (U.S. Patent 5,293,068) and Lin et al. (U.S. Patent 5,239,198).

Applicant has canceled claims 8, 12, 33 and 37.

In summary, Applicant submits that claims 1, 5, 26, and 30 are clearly allowable over the cited prior art for the reasons set forth herein.

Applicant requests the allowance of claims 1, 5, 26, and 30 and the case passed for issue.

Respectfully submitted,

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